REMARKS

These remarks are responsive to the Final Office Action dated January 14, 2004. Claims 1-22 are pending in the present application. Claims 1-8 have been withdrawn from consideration. Claims 9-22 have been rejected. Accordingly, claims 9-22 remain pending.

For the reasons set forth more fully below, Applicant respectfully submits that the present claims are allowable. Consequently, reconsideration, allowance and passage to issue of the present application are respectfully requested.

35 USC §103 Rejections

The Examiner states,

3. Claims 9-12 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ellul et al. in view of Thomas et al.

Regarding claim 9, Ellul et al. (US 5,614,750) teaches a semiconductor device [Figure 6] comprising a substrate 52, a plurality of device structures 90, a buried layer 54, an interconnect comprising a slot 78, a conductive material 82 in the slot, oxidized sidewalls 80 which forms a sinker to the buried layer [column 4, lines 63-67]. Thomas et al. (US 4,933,743) teaches a metal 26 in a slot to form an interconnect. It would have been obvious to one of ordinary skill in the art to use a metal in the device of Ellul et al. since Ellul et al. teaches the use of other conductive materials such as those taught by Thomas et al.

Regarding claims 10-12, Thomas et al. further teaches multiple metals in the interconnect slot which partially fill the slot with a final metal which provides the interconnect layer. It would have been obvious to one of ordinary skill in the art to use the multiple metals of Thomas et al. in the device Ellul et al. since the structure of Thomas et al. provides lower resistance and improved electromigration resistance [column 2, lines 63-67].

Regarding claim 17, Ellul et al. further teaches a sinker coupled to a collector 55.

4. Claims 13-16 and 18-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ellul et al. in view of Thomas et al.

Regarding claim 13, Ellul et al. teaches a semiconductor device [Figure 6] comprising a buried layer 54, an interconnect comprising a slot 78, a conductive material 82 in the slot, oxidized sidewalls 80 which forms a sinker to the buried layer [column 4, lines 63-67]. Thomas et al. teaches a metal 26 in a slot to form an interconnect. It would have been obvious to one of ordinary skill in the art to use a metal in the device of Ellul et al. since Ellul et al. teaches the use of other conductive materials such as those taught by Thomas et al.

Regarding claims 14-16, 20, and 22, Thomas et al. further teaches multiple metals in the interconnect slot which partially fill the slot with a final metal which provides the interconnect

layer where the high current carrying conductors are on the same level [Figure 1L]. It would have been obvious to one of ordinary skill in the art to use the multiple metals of Thomas et al. in the device Ellul et al. since the structure of Thomas et al. provides lower resistance and improved electromigration resistance [column 2, lines 63-67].

Regarding claim 18, Ellul et al. further teaches a slot coupled to the emitter 94.

Regarding claims 19 and 21, Ellul et al. further teaches a CMOS integrated circuit structure with a bipolar device. Thomas et al. teaches an integrated circuit with bipolar and MOS logic circuits on the same device [column 1, lines 12-25]. It would have been obvious to one of ordinary skill in the art to use the device of Ellul et al. in an IC comprising bipolar transistors and MOS transistors since these are well known in the art as devices integrated on the same circiut using high voltage interconnects.

Applicant respectfully disagrees.

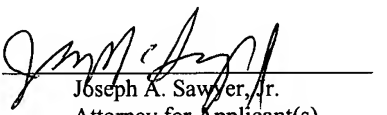
All of the independent claims include an interconnect comprising at least one slot . . . and at least one metal within the slot." As the Examiner has pointed out, Ellul discloses a trench which includes polysilicon. This is clearly different from the metal within the slot, as recited in the present invention. Since the interconnect includes metal the interconnect can be utilized in high voltage applications. Thomas teaches an interconnect system but neither includes or suggests connecting that system to a buried layer to form a sinker. The slots provide oxide isolation which allows for closer spacing, lower leakage, lower capacitance. The polysilicon layer disclosed in Ellul would not provide such advantages and Thomas only teaches the use of an interconnect system on top of the substrate. Accordingly, for these reasons claims 9-22 are allowable over the cited reference.

Applicant's attorney believes that this application is in condition for allowance. Should any unresolved issues remain, Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,

SAWYER LAW GROUP LLP

March 15, 2004
Date



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